UTILITY
PATENT APPLICATION
TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	**2666.43**
First Named Inventor or Application Identifier	
	SAEED AZIMI
Express Mail Label No.	

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. [X] Specification   *Total Pages* [28]

3. [X] Drawing(s) *(35 USC 113)*   *Total Sheets* [5]

4. [X] Oath or Declaration *Total Pages* [2]

   a. [X] Newly executed (original or copy)

   b. [ ] Unexecuted for information purposes

   c. [ ] Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]

     i. [ ] <u>DELETION OF INVENTOR(S)</u>
Signed Statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation By Reference *(useable if Box 4c is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4c, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)

   a. [ ] Computer Readable Copy

   b. [ ] Paper Copy (identical to computer copy)

   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))

9. [ ] 37 CFR 3.73(b) Statement
(when there is an assignee)   [ ] Power of Attorney

10. [ ] English Translation Document *(if applicable)*

11. [ ] Information Disclosure Statement (IDS)/PTO-1449   [ ] Copies of IDS Citations

12. [ ] Preliminary Amendment

13. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

14. [X] Small Entity Statement(s)   [ ] Statement filed in prior application Status still proper and desired

15. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)

16. [ ] Other: _____

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*

[ ] Continuation   [ ] Divisional   [ ] Continuation-in-part (CIP)   of prior application No. ___/_____

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label   05514 (Insert Customer No. or Attach bar code label here)   or [ ] Correspondence address below

NAME	
Address	

City		State		Zip Code	
Country		Telephone		Fax	

| CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	75 -20 =	55	X $ 18.00 =	$990.00
	INDEPENDENT CLAIMS (37 cfr 1.16(b))	15 -3 =	12	X $ 78.00 =	$936.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			$260.00 =	$000.00
				BASIC FEE (37 CFR 1.16(a))	$690.00
				Total of above Calculations =	$2,616.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				$1,308.00
				TOTAL =	$1,308.00

19. Small entity status

 a. [X] A Small entity statement is enclosed

 b. [ ] A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.

 c. [ ] Is no longer claimed.

20. [X] A check in the amount of $ 1,308.00 for the filing fee is enclosed.

21. [X] Two (2) checks in the amount of $ 40.00 each to cover the recordal fee for two Assignments are enclosed.

22. The Commissioner is hereby authorized to credit any overpayments or charge any deficiencies to Deposit Account No. 06-1205:

 a. [X] Fees required under 37 CFR 1.16.

 b. [ ] Fees required under 37 CFR 1.17.

 c. [ ] Fees required under 37 CFR 1.18.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	RICHARD P. BAUER, REG. NO. 31,588
SIGNATURE	
DATE	September 14, 2000

STATEMENT CLAIMING SMALL ENTITY STATUS   DOCKET NUMBER
(37 CFR 1.9(f) & 1.27(c)—SMALL BUSINESS CONCERN   MP0043

Applicant, Patentee, or Identifier:
Application or Patent No.
Filed or Issued: September 14, 2000
Title: Long Latency Interface Between Hardware Components

I hereby state that I am
_____   the owner of the small business concern identified below:
__X__   an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF SMALL BUSINESS CONCERN: Marvell Technology Group Ltd.
ADDRESS OF SMALL BUSINESS CONCERN: Richmond House, 3rd floor, 12 Parla Ville Road, Hamilton HM DX, Bermuda.

        I hereby state that the above identified small business concern qualifies as a small business concern as defined in 13 CFR Part 121 for purposes of paying reduced fees to the United States Patent and Trademark Office. Questions related to size standards for a small business concern may be directed to: Small Business Administration, Size Standards Staff, 409 Third Street, SW, Washington, DC 20416.

        I hereby state that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

__X__ -   the specification filed herewith with title as listed above.
_____   the application identified above.
_____   the patent identified above.

        If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate statements as to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

        Each person, concern, or organization having any rights in the invention is listed below·
__X__   no such person, concern, or organization exists.
_____   each such person, concern, or organization is listed below.

        Separate statements are required from each named person, concern or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

        I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

NAME OF PERSON SIGNING _____ Eric Janofsky _____

TITLE OF PERSON IF OTHER THAN OWNER _____ General Patent Counsel _____

ADDRESS OF PERSON SIGNING 645 Almanor Avenue _____
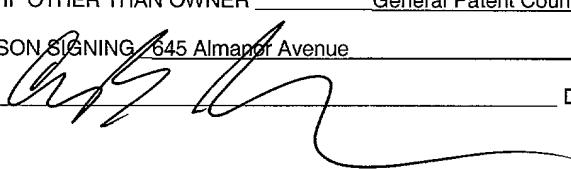
SIGNATURE _____ DATE _____ 09/13/00 _____

HIGH LATENCY INTERFACE BETWEEN
HARDWARE COMPONENTS

Cross-Reference to Related Applications

This application claims priority under 35 U.S.C. § 119(e) on U.S. provisional application serial no. 60/205,594, entitled "High Latency RDC/HDC Interface," filed May 17, 2000, the contents of which are incorporated by reference herein.

Field of the Invention

The present invention relates to a versatile, latency-independent interface between hardware components, such as between a read/write (R/W) channel or read channel (RDC) and a hard disk controller (HDC). Such an interface is flexible enough to support high read and write latencies of greater than one sector, a split sector format, and a second sector mark.

Background of the Invention

As is shown in Fig. 1, a typical disk drive system includes a hard disk controller (HDC) 12 that interfaces with a R/W channel or RDC 14 which is in communication with a disk 16. Data transfer between the HDC and the R/W channel is synchronized by read gate (RGATE) and write gate (WGATE) control signals. In a read operation, R/W channel 14 processes an incoming analog signal from disk 16 and transfers the data to HDC 12. In a write operation, data is transferred from the HDC to the R/W channel to be written to the disk. Latency refers to the time or byte delay that data remains in the R/W channel. Some disk drive systems have latencies of about 20 bytes which, depending on the

particular system, amounts to a time delay of between about 800 ns and 5 ms.

Technology such as iterative turbo coding, which is being introduced into modern disk drive systems, requires more processing before the data is available, which, in turn, requires R/W channels or RDCs with higher latencies. One problem is that the interface used in the shorter latency systems is not capable of supporting the higher latencies. Accordingly, a new interface is needed that supports higher latency R/W channel or RDC designs.

Summary of the Invention

It is therefore an object of the present invention to provide an interface between hardware components, such as between an HDC and a R/W channel or RDC, that supports relatively high read and write latencies.

It is another object of this invention to provide an interface signaling protocol which is flexible enough to support high read and write latencies of greater than one sector, and which supports a split sector format and multiple sector marks.

According to one aspect of the invention, a latency-independent interface between first and second hardware components is provided. Such a latency-independent interface comprises a data gate circuit that transmits a data gate signal; a data circuit that transmits or receives data under the control of the data gate signal; a media gate circuit that transmits a media gate signal; a mode selection circuit that transmits mode selection information under the control of the media gate signal; and a buffer attention circuit that receives a buffer attention signal.

In another aspect, the invention involves a latency-independent interface between first and second hardware

components, which comprises a data gate circuit that receives a data gate signal; a data circuit that transmits or receives data under the control of the data gate signal; a media gate circuit that receives a media gate signal; a mode selection circuit that

5   receives mode selection information under the control of the media gate signal; and a buffer attention circuit that transmits a buffer attention signal.

In yet another aspect of the invention, a latency-independent interface between first and second hardware

10   components is provided. Such a latency-independent interface comprises a first data gate circuit that transmits a data gate signal; a first data circuit that transmits or receives data under the control of the data gate signal; a first media gate circuit that transmits a media gate signal; a first mode

15   selection circuit that transmits mode selection information under the control of the media gate signal; a first buffer attention circuit that receives a buffer attention signal; a second data gate circuit that receives the data gate signal; a second data circuit that transmits or receives data under the

20   control of the data gate signal; a second media gate circuit that receives the media gate signal; a second mode selection circuit that receives mode selection information under the control of the media gate signal; and a second buffer attention circuit that transmits a buffer attention signal.

25   Preferably, the mode selection information comprises tag information and control information. More preferably, the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from

30   a previous location or from a new location, a reset command, and size information including a size command that indicates size of associated data.

In other aspects, the invention embraces methods of transmitting and receiving signals between first and second hardware components corresponding to each of the interface devices set forth above. Such methods and/or steps thereof may

5 be implemented by a program of instructions (e.g., software) embodied on a device-readable medium, such as a magnetic tape or disk, or optical medium that may be used to store such instructions. More broadly, the device-readable medium may include signals transmitted over network paths, infrared

10 signals, as well as other signals throughout the electromagnetic spectrum that may be used to convey instructions. The instructions may be executed by a computer or other processor-controlled device. The program of instructions may also be in the form of hardware, or combination of software and hardware.

15 Still other aspects of the invention include interface protocols between at least two hardware components corresponding to each of the interface devices set forth above.

Other objects and attainments together with a fuller understanding of the invention will become apparent and

20 appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a block diagram of a conventional RDC/HDC

25 interface.

Fig. 2 is a block diagram of an interface between two hardware components, such as an HDC and an RDC or R/W channel, in accordance with embodiments of the invention.

Fig. 3 is a timing diagram for write/read operations, in

30 accordance with embodiments of the invention.

Figs. 4(a), (b) and (c) are timing diagrams for high latency write operation, in accordance with embodiments of the invention.

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Figs. 5(a), (b) and (c) are timing diagrams for high latency read operation, in accordance with embodiments of the invention.

Detailed Description of the Invention

5   Referring to Fig. 2, a block diagram of an interface 20 between a first hardware component 22 and a second hardware component 24, in accordance with embodiments of the invention, is illustrated. In a preferred embodiment, first hardware component 22 is a hard disk controller (HDC) and second hardware component

10   14 is a read/write (R/W) channel or read channel (RDC), although the invention is not so limited. Rather, interface 20 of the present invention may be employed in connection with other suitable functional hardware components between which data is transferred.

15   In accordance with the invention, interface 20 employs a new signaling protocol which decouples the timing of the conventional read and write gate control signals with the transfer of data by replacing those signals with a MediaGate signal, as described below. The interface supports read and write latencies of more

20   than a sector long. The interface also supports split sector format (i.e., noncontiguous sectors of data) and multiple sector marks.

    In the illustrated embodiment, the interface 20 of the present invention employs a read clock signal (RCLK) sourced from

25   the R/W channel and output during read operations, and a write clock signal (WCLK) sourced from the HDC and output during write operations.

    In accordance with the invention, interface 20 further includes two buses and two respectively associated control

30   signals. A data gate signal (DataGate), sourced from the HDC, is synchronous with, and controls, NRZ data transfer between the R/W channel and the HDC via a bi-directional data bus. In one

embodiment, the data bus (NRZ [7:0]) is byte-wide, with bits 0 –
7 represented by NRZ [0] – NRZ [7]. However, the data bus of the
present invention may accommodate more or less than eight bits.
The data signal may also include a parity bit, which in a byte-
wide signal may be represented by NRZ [8].

A media gate signal (MediaGate) is provided which, as
previously noted, replaces the conventional read and write gate
control signals. MediaGate is sourced from the HDC and indicates
the location of particular sectors on the track media. MediaGate
is used to control data transfer between the disk and the R/W
channel and is associated with a mode selection bus MCMD [1:0]
that provides mode selection information to the R/W channel.
Such mode selection information includes tag, control and size
information. More specifically, such mode selection information
includes commands such as "Tag ID" that identifies the sector in
which the associated data is contained, "Cont" or "New" which
indicates that the data is continued from the previous sector or
from a new sector and "Reset" which resets the data transfer
operation, and "Size" which indicates the byte size of the data
of bytes.

Another interface signal, FIFOattn, is sourced from the R/W
channel and indicates channel FIFO status during write and read
operations. When the channel FIFO becomes full during a write
operation, FIFOattn is asserted (i.e., becomes high) to indicate
that the channel FIFO is full and that no more data can be
transferred from HDC at this time. In that situation, the HDC
must pause and resume data transfer only after FIFOattn is de-
asserted. During read operation, a high FIFOattn indicates that
the channel FIFO is ready for data from the HDC. On the other
hand, a low FIFOattn indicates that no data can be transferred,
in which case the HDC must pause data transfer until FIFOattn is
asserted.

Each of the HDC 22 and the R/W channel 24 include appropriate circuitry for transmitting and receiving the various signals, data and mode selection information between the two hardware components. For example, HDC 22 includes a data gate circuit 32 that transmits DataGate, and a data circuit 34 that transmits and receives data on the data bus under the control of DataGate. HDC 22 also includes a media gate circuit 36 that transmits MediaGate, and a mode selection circuit 38 that transmits mode selection information under the control of MediaGate. A buffer attention circuit 39 is provided for receiving FIFOattn. R/W channel 24 comprises corresponding circuit components, including a data gate circuit 42 that receives DataGate, and a data circuit 44 that transmits and receives data on the data bus under the control of DataGate. R/W channel 24 also includes a media gate circuit 46 that receives MediaGate, and a mode selection circuit 48 that receives mode selection information under the control of MediaGate. A buffer attention circuit 49 is provided for transmitting FIFOattn. Signal and data transmitting and receiving circuits are generally known, and based on the teachings provided herein, one skilled in the art would be able to construct and implement transmitting and receiving circuits to carry out the specific signaling protocol described herein.

A parity signal (not shown), sourced from the R/W channel, may be used during write mode as a parity error feedback for write data input. During read mode, the parity signal can be used to output a Thermal Asperity (TA) detector's flag.

Fig. 3 is an exemplary timing diagram for write/read operations. Timing of the control signal MediaGate and its associated bus MCMD [1:0] are illustrated, along with WCLK.

In write/read operations, according to one embodiment, the R/W channel samples MCMD [1:0], received from the HDC, eight

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times in accordance with the WCLK/RCLK immediately after MediaGate is asserted. There are 2 bits/sample making a total of 16 bits. The R/W channel decodes the 16 bits of mode selection commands from the most significant bit to the least significant bit as set forth in Table 1 below.

Bits	Command	Description
MCMD [15:13]	Tag	3 bits of Tag information (0 - 7)
MCMD [12]	Reset	1 = Reset Used for Read only
MCMD [11]	New/Cont	0 = new sector 1 = continue previous sector
MCMD [10:0]	Size	Size in resolution of 4 bytes up to a maximum size of 8 Kbytes

Table 1

In addition to the commands listed in Table 1, commands indicating various error conditions may also be employed.

In write/read operations, the assertion of DataGate is synchronous with NRZ data transfer. The 5 lower bits of the conventional Sync byte are replaced with data command information (DCMD) on the data bus NRZ [7:0]. The R/W channel decodes the lower 5 bits of DCMD as set forth below in Table 2.

Bits	DCMD	Description
DCMD [4:2]	Tag	3 bits of Tag information (0 - 7)
DCMD [1]	Reset	1 = Reset Used for Write only
DCMD [0]	New/Cont	0 = new sector 1 = continue previous sector

Table 2

In addition to the commands listed in Table 2, a size command may also be used.

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Regarding the operation of FIFOattn, for write operations, FIFOattn will be asserted by the R/W channel just before its FIFO becomes full. In particular, after FIFOattn is asserted (i.e., goes high), the R/W channel FIFO is able to accept one more byte from the HDC. After that, while FIFOattn remains high, the HDC assumes a pause state and does not resume data transfer until FIFOattn is de-asserted again.

For read operations, FIFOattn will be asserted by the R/W channel if its FIFO data is available to be transferred to the HDC. After FIFOattn is de-asserted (i.e., goes from high to low), the HDC can read one more byte of data. After that, while FIFOattn remains low indicating the R/W channel FIFO is not ready, the HDC assumes a pause state. Data transfer from the R/W channel to the HDC is not resumed until FIFOattn is asserted again.

Write Operation

A write operation is initiated by the HDC by asserting DataGate which is synchronous with the data transfer on NRZ [7:0]. The NRZ data is latched by the R/W channel on the rising edge of WCLK, as shown in Fig. 4. HDC provides additional mode selection commands (DCMD) using the lower 5 bits of the sync byte. The values of DCMD are set forth above in Table 2.

Fig. 4(a) illustrates the overall timing of signals including the interface signals in the write operation. The servo signal indicates where positioning information is located to maintain the center of the disk sensing element over a center of a track on the disk 16. The data is written on a specific track of the disk, and the track signal contains that information in a specific format required by the RDC. Fig. 4(b) is a "blow up" of that portion of Fig. 4(a) showing MCMD information transfer which occurs over the "PLO" field which is the period that RDC acquires phase lock to the incoming track signal. Fig.

4(c) is a "blow up" of that portion of Fig. 4(a) illustrating DCMD transfer which occurs over the beginning of the data transfer between HDC and RDC indicated by the rising edge of the DataGate signal.

In the case where the R/W channel FIFO is becoming full, with the high latency R/W channel of the present invention, FIFOattn will be asserted by the R/W channel when its FIFO has only one more location for data before it reaches an overflow condition. After detecting FIFOattn, HDC enters a pause state in which data transfer is temporarily halted. Data transfer is resumed only after FIFOattn is de-asserted. When data transfer is resumed the HDC also provides appropriate mode selection commands (DCMD).

The HDC provides additional information to the R/W channel on MediaGate, MCMD0 and MCMD1. After receiving the size information and matching the Tag IDs (DCMD and MCMD tag fields), the R/W channel can write data to the medium (e.g., the disk). The "New" command is issued for the beginning of a sector of data, while "Cont" is issued for the remaining data of a split sector. The HDC may use the "Reset" command to reset/reinitialize the R/W channel FIFO pointer.

Read Operation

Exemplary timing diagrams of various signals employed in high latency read operation is illustrated in Fig. 5. Fig. 5(a) illustrates the overall timing of signals including the interface signals in the read operation. The servo signal and track signal function as explained above. Fig. 5(b) is a "blow up" of that portion of Fig. 5(a) showing MCMD information transfer which occurs over the "PLO" field which is the period that RDC acquires phase lock to the incoming track signal. Fig. 5(c) is a "blow up" of that portion of Fig. 5(a) illustrating DCMD transfer which

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occurs over the beginning of the data transfer between HDC and RDC indicated by the rising edge of the DataGate signal.

The R/W channel can read data from the medium, after receiving the size information and the "New" or "Cont" command. With the high latency R/W channel of the present invention, FIFOattn will be asserted by the R/W channel if its FIFO is ready to transfer data. The HDC starts receiving data after detecting FIFOattn in the asserted state. The R/W channel de-asserts FIFOattn one byte of data before an underrun condition occurs. After FIFOattn is de-asserted, the HDC enters a pause state in which data is not received. The R/W channel provides DCMD information when asserting FIFOattn again to allow data transfer to continue.

In transferring data from the R/W channel to the HDC with DCMD, the NRZ data is latched by the HDC on each rising edge of RCLK. The R/W channel provides an additional byte of mode information (DCMD) before regular data transfer. The DCMD values are set forth in Table 2 above. The R/W channel may use the Reset command to inform the HDC to reset/re-initialize the memory.

The interface signaling protocol of the present invention may be controlled by a processor operating in accordance with a program of instructions which may be in the form of software. Alternatively, the program of instructions may be implemented with discrete logic components, application specific integrated circuits (ASICs), digital signal processors, or the like. Based on the teachings herein, one skilled in the art would be able to implement an appropriate instruction program in either software or hardware for carrying out the interface signaling protocol of the present invention.

It should be readily apparent from the foregoing description that the interface of the present invention supports

high read and write latencies of greater than one sector. In particular, with the additional Tag ID and control bits, interface 20 can support an R/W channel latency more than one sector long. The Tag ID advantageously allows the transfer of multiple noncontiguous sectors or out-of-order sectors. Moreover, the interface is also capable of supporting a split sector format and a multiple sector mark.

While embodiments of the invention have been described, it will be apparent to those skilled in the art in light of the foregoing description that many further alternatives, modifications and variations are possible. The invention described herein is intended to embrace all such alternatives, modifications and variations as may fall within the spirit and scope of the appended claims.

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WHAT IS CLAIMED IS:

1.   A   latency-independent   interface   between   first   and
second hardware components, comprising:

a data gate circuit that transmits a data gate signal;

5   a data circuit that transmits or receives data under
the control of the data gate signal;

a media gate circuit that transmits a media gate
signal;

a mode selection circuit that transmits mode selection

10   information under the control of the media gate signal; and

a buffer attention circuit that receives a buffer
attention signal.

2.   The latency-independent interface of claim 1, wherein

15   the mode selection information comprises tag information and
control information.

3.   The latency-independent interface of claim 2, wherein
the tag information comprises a tag command that identifies a

20   location   of   associated   data,   and   the   control   information
comprises commands that indicate whether associated data is
continued from a previous location or from a new location.

4.   The latency-independent interface of claim 3, wherein

25   the control information further comprises a reset command.

5.   The latency-independent interface of claim 3, wherein
the control information further comprises size information
comprising a size command that indicates size of associated

30   data.

6. A latency-independent interface between first and second hardware components, comprising:

a data gate circuit that receives a data gate signal;

a data circuit that transmits or receives data under the control of the data gate signal;

a media gate circuit that receives a media gate signal;

a mode selection circuit that receives mode selection information under the control of the media gate signal; and

a buffer attention circuit that transmits a buffer attention signal.

7. The latency-independent interface of claim 6, wherein the mode selection information comprises tag information and control information.

8. The latency-independent interface of claim 7, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

9. The latency-independent interface of claim 8, wherein the control information further comprises a reset command.

10. The latency-independent interface of claim 8, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

11. A latency-independent interface between first and second hardware components, comprising:

a first data gate circuit that transmits a data gate signal;

a first data circuit that transmits or receives data under the control of the data gate signal;

a first media gate circuit that transmits a media gate signal;

a first mode selection circuit that transmits mode selection information under the control of the media gate signal;

a first buffer attention circuit that receives a buffer attention signal;

a second data gate circuit that receives the data gate signal;

a second data circuit that transmits or receives data under the control of the data gate signal;

a second media gate circuit that receives the media gate signal;

a second mode selection circuit that receives mode selection information under the control of the media gate signal; and

a second buffer attention circuit that transmits a buffer attention signal.

12. The latency-independent interface of claim 11, wherein the mode selection information comprises tag information and control information.

13. The latency-independent interface of claim 12, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

14. The latency-independent interface of claim 13, wherein the control information further comprises a reset command.

5   15. The latency-independent interface of claim 13, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

10   16. A latency-independent interface between first and second hardware components, comprising:

data gate circuit means for transmitting a data gate signal;

data circuit means for transmitting or receiving data under the control of the data gate signal;

media gate circuit means for transmitting a media gate signal;

mode selection circuit means for transmitting mode selection information under the control of the media gate signal; and

buffer attention circuit means for receiving a buffer attention signal.

17. The latency-independent interface of claim 16, wherein
25   the mode selection information comprises tag information and control information.

18. The latency-independent interface of claim 17, wherein the tag information comprises a tag command that identifies a
30   location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

19. The latency-independent interface of claim 18, wherein the control information further comprises a reset command.

5   20. The latency-independent interface of claim 18, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

10   21. A latency-independent interface between first and second hardware components, comprising:

data gate circuit means for receiving a data gate signal;

data circuit means for transmitting or receiving data under the control of the data gate signal;

media gate circuit means for receiving a media gate signal;

mode selection circuit means for receiving mode selection information under the control of the media gate signal; and

buffer attention circuit means for transmitting a buffer attention signal.

22. The latency-independent interface of claim 21, wherein
25   the mode selection information comprises tag information and control information.

23. The latency-independent interface of claim 22, wherein the tag information comprises a tag command that identifies a
30   location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

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24. The latency-independent interface of claim 23, wherein the control information further comprises a reset command.

5   25. The latency-independent interface of claim 23, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

10   26. A latency-independent interface between first and second hardware components, comprising:

first data gate circuit means for transmitting a data gate signal;

first data circuit means for transmitting or receiving data under the control of the data gate signal;

15   first media gate circuit means for transmitting a media gate signal;

first mode selection circuit means for transmitting mode selection information under the control of the media gate signal;

20   first buffer attention circuit means for receiving a buffer attention signal;

second data gate circuit means for receiving the data gate signal;

25   second data circuit means for transmitting or receiving data under the control of the data gate signal;

second media gate circuit means for receiving the media gate signal;

second mode selection circuit means for receiving mode

30   selection information under the control of the media gate signal; and

second buffer attention circuit means for transmitting a buffer attention signal.

27. The latency-independent interface of claim 26, wherein the mode selection information comprises tag information and control information.

28. The latency-independent interface of claim 27, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

29. The latency-independent interface of claim 28, wherein the control information further comprises a reset command.

. 30. The latency-independent interface of claim 28, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

31. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:
transmitting a data gate signal;
transmitting or receiving data under the control of the data gate signal;
transmitting a media gate signal;
transmitting mode selection information under the control of the media gate signal; and
receiving a buffer attention signal.

32. The method of claim 31, wherein the mode selection information comprises tag information and control information.

33. The method of claim 32, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

34. The method of claim 33, wherein the control information further comprises a reset command.

35. The method of claim 33, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

36. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

    receiving a data gate signal;

    transmitting or receiving data under the control of the data gate signal;

    receiving a media gate signal;

    receiving mode selection information under the control of the media gate signal; and

    transmitting a buffer attention signal.

37. The method of claim 36, wherein the mode selection information comprises tag information and control information.

38. The method of claim 37, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that

indicate whether associated data is continued from a previous location or from a new location.

39. The method of claim 38, wherein the control information further comprises a reset command.

40. The method of claim 38, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

41. A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting and receiving a data gate signal;

transmitting or receiving data under the control of the data gate signal;

transmitting and receiving a media gate signal;

transmitting and receiving mode selection information under the control of the media gate signal; and

transmitting and receiving a buffer attention signal.

42. The method of claim 41, wherein the mode selection information comprises tag information and control information.

43. The method of claim 42, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

44. The method of claim 43, wherein the control information further comprises a reset command.

45. The method of claim 43, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

46. An interface protocol between at least two hardware components, comprising:

a transmitted data gate signal;

a data signal carrying data that is transmitted or received under the control of the data gate signal;

a transmitted media gate signal;

a mode selection signal carrying mode selection information that is transmitted under the control of the media gate signal; and

a received buffer attention signal.

47. The interface protocol of claim 46, wherein the mode selection information comprises tag information and control information.

48. The interface protocol of claim 47, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

49. The interface protocol of claim 48, wherein the control information further comprises a reset command.

50. The interface protocol of claim 48, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

51. An interface protocol between at least two hardware components, comprising:

a received data gate signal;

a data signal carrying data that is transmitted or received under the control of the data gate signal;

a received a media gate signal;

a mode selection signal carrying mode selection information that is received under the control of the media gate signal; and

a transmitted buffer attention signal.

52. The interface protocol of claim 51, wherein the mode selection information comprises tag information and control information.

53. The interface protocol of claim 52, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

54. The interface protocol of claim 53, wherein the control information further comprises a reset command.

55. The interface protocol of claim 53, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

56. An interface protocol between at least two hardware components, comprising:

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a data gate signal transmitted by a first hardware component and received by a second hardware component;

a data signal that transmits data between the first and second hardware components under the control of the data gate signal;

a media gate signal transmitted by the first hardware component and received by the second hardware component;

a mode selection signal that transmits mode selection information from the first hardware component to the second hardware component under the control of the media gate signal; and

a buffer attention signal transmitted by the second hardware component and received by the first hardware component.

57. The interface protocol of claim 56, wherein the mode selection information comprises tag information and control information.

58. The interface protocol of claim 57, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

59. The interface protocol of claim 58, wherein the control information further comprises a reset command.

60. The interface protocol of claim 58, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

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61. A device-readable medium embodying a program of instructions for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program of instructions comprising instructions for:

       transmitting a data gate signal;

       transmitting or receiving data under the control of the data gate signal;

       transmitting a media gate signal;

       transmitting mode selection information under the control of the media gate signal; and

       receiving a buffer attention signal.

62. The device-readable medium of claim 61, wherein the mode selection information comprises tag information and control information.

63. The device-readable medium of claim 62, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

64. The device-readable medium of claim 63, wherein the control information further comprises a reset command.

65. The device-readable medium of claim 63, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

66. A device-readable medium embodying a program of instructions for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program of instructions comprising

5   instructions for:

receiving a data gate signal;

transmitting or receiving data under the control of the data gate signal;

receiving a media gate signal;

10   receiving mode selection information under the control of the media gate signal; and

transmitting a buffer attention signal.

67. The device-readable medium of claim 66, wherein the mode selection information comprises tag information and control

15   information.

68. The device-readable of claim 67, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises

20   commands that indicate whether associated data is continued from a previous location or from a new location.

69. The device-readable medium of claim 68, wherein the

25   control information further comprises a reset command.

70. The device-readable medium of claim 68, wherein the control information further comprises size information comprising a size command that indicates size of associated

30   data.

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71. A device-readable medium embodying a program of instructions for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program of instructions comprising

5   instructions for:

transmitting and receiving a data gate signal;

transmitting or receiving data under the control of the data gate signal;

transmitting and receiving a media gate signal;

10   transmitting and receiving mode selection information under the control of the media gate signal; and

transmitting and receiving a buffer attention signal.

72. The device-readable medium of claim 71, wherein the mode selection information comprises tag information and control

15   information.

73. The device-readable medium of claim 72, wherein the tag information comprises a tag command that identifies a

20   location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

74. The device-readable medium of claim 73, wherein the

25   control information further comprises a reset command.

75. The device-readable medium of claim 73, wherein the control information further comprises size information comprising a size command that indicates size of associated

30   data.

ABSTRACT

A latency-independent interface between hardware components, such as a hard disk controller (HDC) and a read/write (R/W) channel or a read channel (RDC) supports high read and write latencies of greater than one sector. Such an interface also supports a split sector format and multiple mark format. In addition to read and write clock signals, the interface comprises a data gate signal that controls the transfer of data between the the HDC and R/W channel, and a media gate signal that controls transfer of mode selection information from the HDC to the R/W channel and also controls the transfer of data between the R/W channel and a disk. The media gate signal replaces the conventional read and write gate control signals. A buffer attention signal is also provided.

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Fig. 1

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HDC		R/W channel or RDC
	32 → DataGate → 42	
	38 ⟹ MCMD [1:0] ⟹ 48	
	39 ← FIFOattn ← 49	
	36 → MediaGate → 46	
	→ WCLK →	
	← RCLK ←	
	34 ⟷ NRZ [7:0] ⟷ 44	
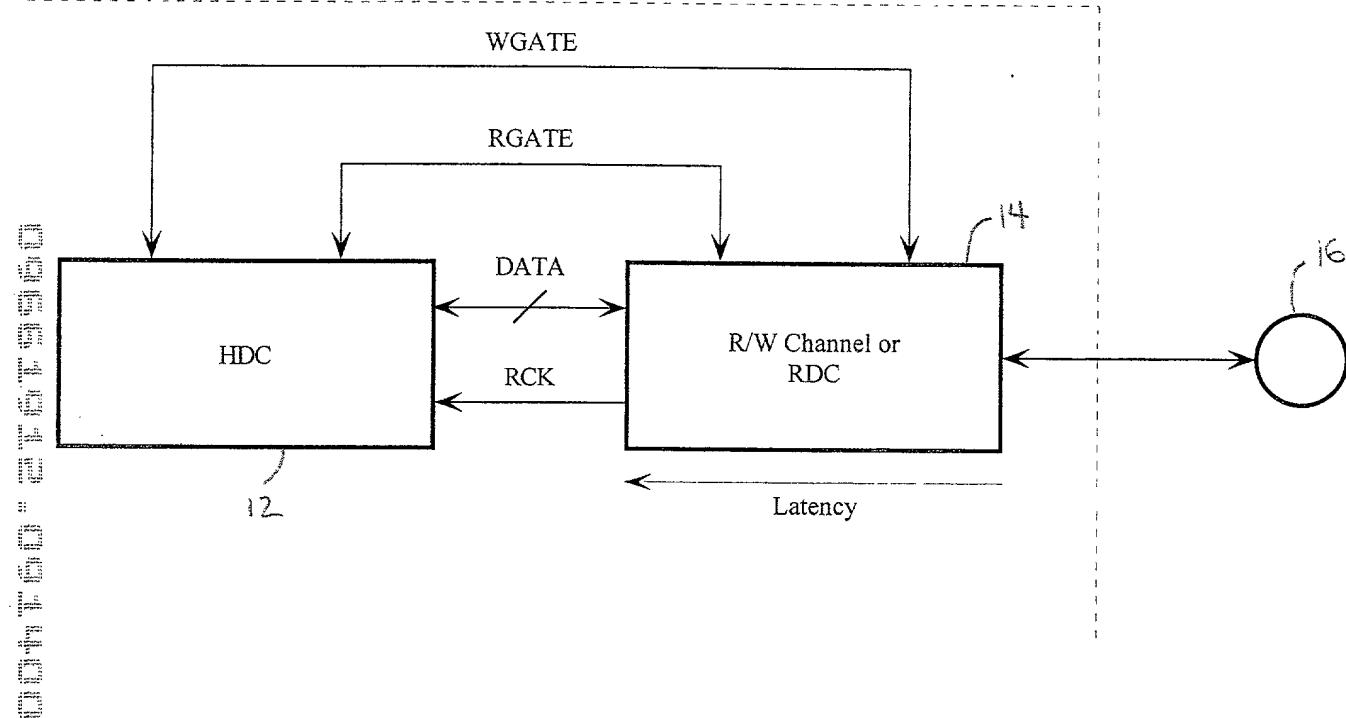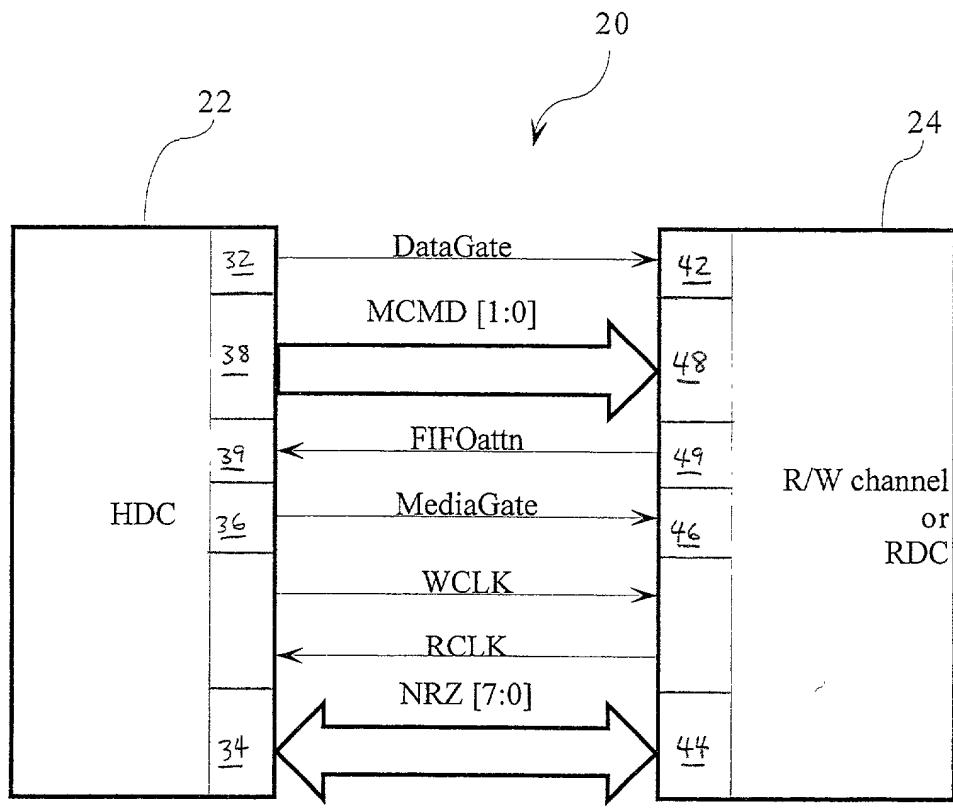
Fig. 2

MV Interface Description
This interface uses additional pins to provide Tag/mode selection info for future implementations of high
latency RDC designs with latency could be more than one sector long

**MCMD timing chart for Write/Read operations**

Fig. 3

High latency write

(c)

Servo

Track

MediaGate

MCMD [1:0]

WCLK

DataGate

FIFOattn

NRZ — ⟨DCMD⟩⟨D0⟩⟨D1⟩⟨D2⟩————⟨DCMD⟩⟨D3⟩⟨D4⟩⟨D5⟩

(b)

Servo

Track ——————————⟨ PLO ⟩

MediaGate

MCMD [1:0] ——⟨M[15:14]⟩⟨M[13:12]⟩⟨M[11:10]⟩⟨M[9:8]⟩⟨M[7:6]⟩⟨M[5:4]⟩⟨M[3:2]⟩⟨M[1:0]⟩

WCLK

DataGate

FIFOattn

NRZ

(a)

Servo

Track —————⟨ PLO ⟩⟨USER DATA⟩⟨USER DATA⟩⟨PAD⟩——⟨SW⟩⟨SECTOR 3⟩

MediaGate

MCMD[1:0]

WCLK

DataGate

FIFOattn

NRZ
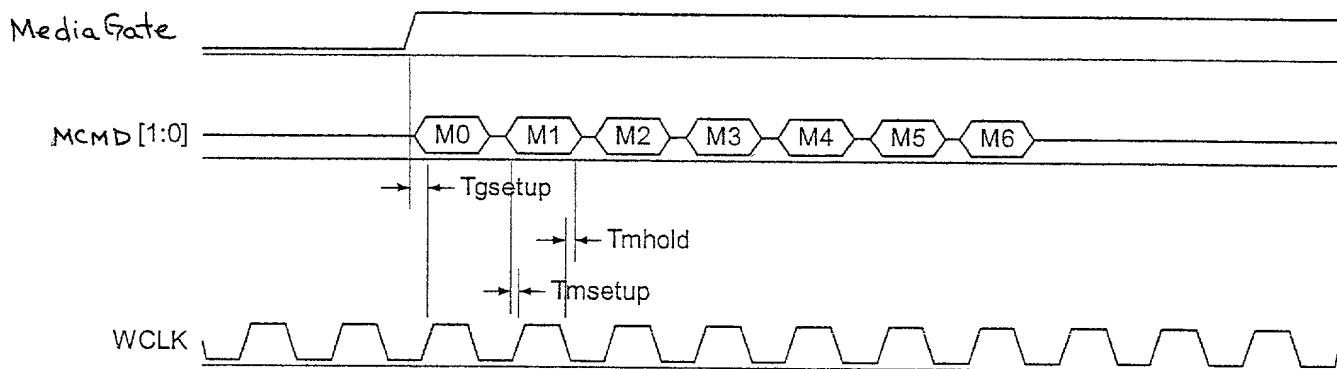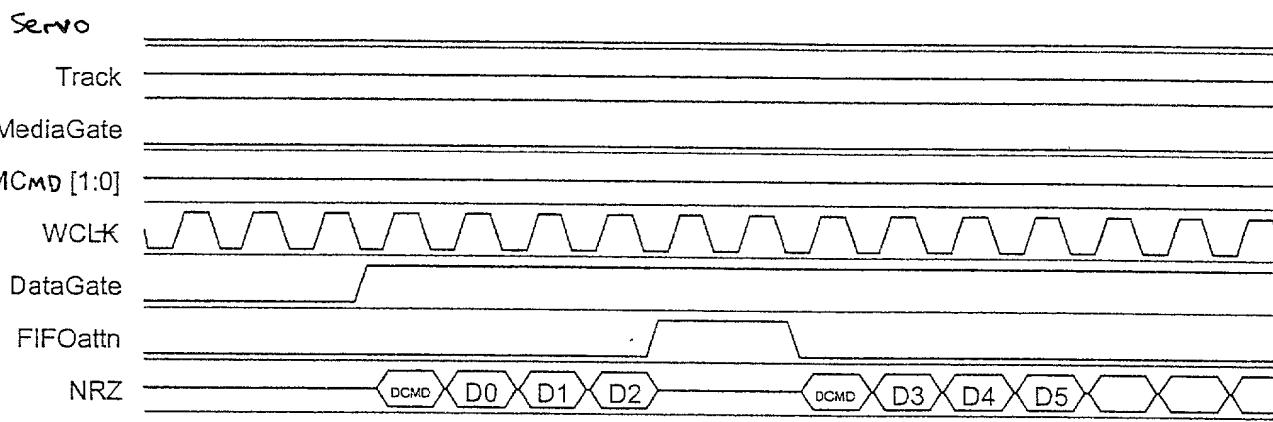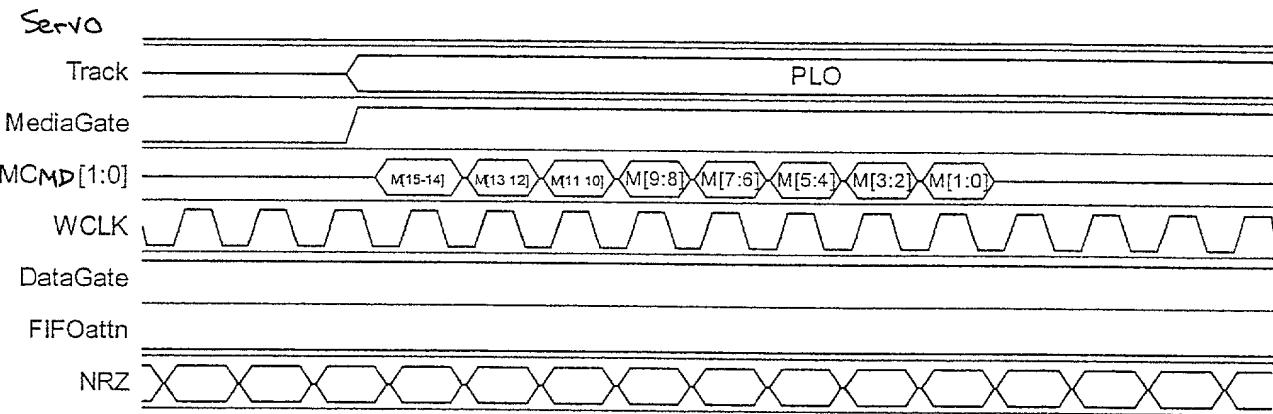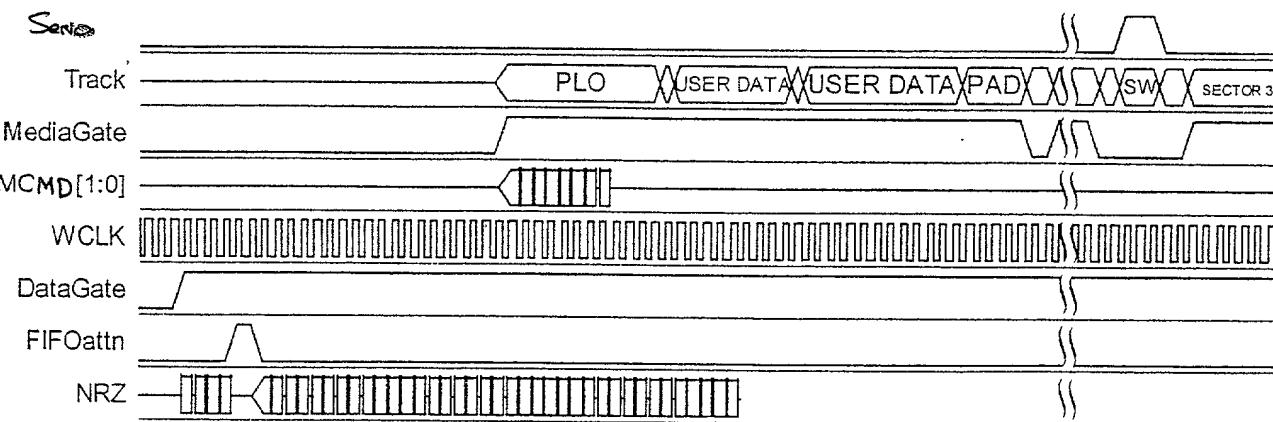
Fig. 4
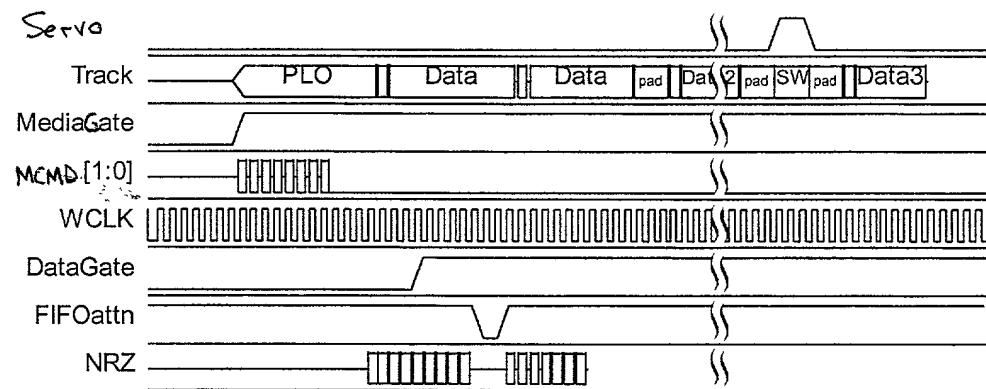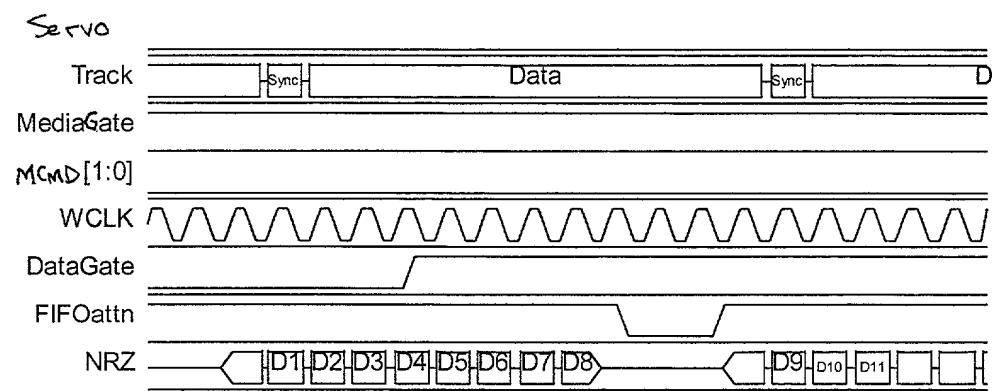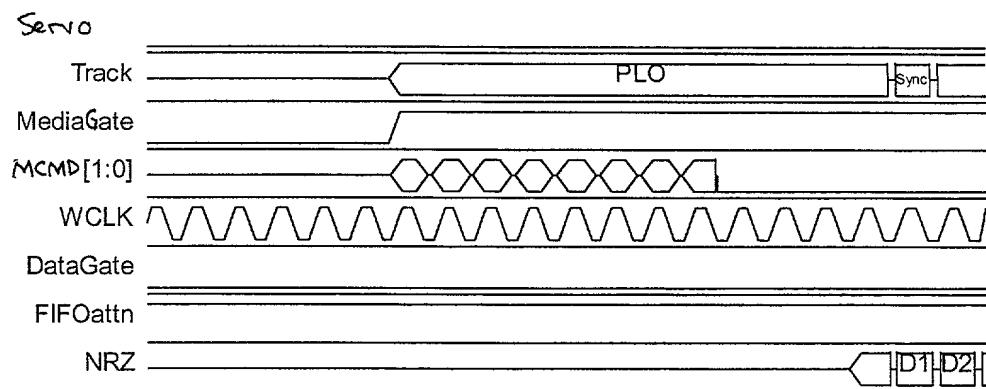
Fig. 5

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
(Page 1)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **Long Latency Interface Between Hardware Components**

the specification of which is attached hereto X was filed on __ as United States Application No. or PCT International Application No. _
and was amended on_____ _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR ' 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. ' 119(a)-(d) or ' 365(b), of any foreign application(s) for patent or inventor's certificate, or ' 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	(Yes/No) Priority Claimed

I hereby claim the benefit under 35 U.S.C. ' 119(e) of any United States provisional application(s) listed below:

Application No.	Filed (Day/Mo./Yr.)
60/205,594	May 17, 2000

I hereby claim the benefit under 35 U.S.C. ' 120 of any United States application(s), or ' 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. ' 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. ' 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

		Status
Application No.	Filed (Day/Mo./Yr.)	(Patented, Pending, Abandoned)

I hereby appoint the practitioners associated with the firm and Customer Number provided below and Eric B. Janofsky, Reg. No. 30,759 to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole or First Inventor **Azimi, Saeed**

Inventor's signature _____

Date September 13, 2000 _____ Citizen/Subject of **United States of America**

Residence 4820 **Cabello Court , Union City, CA, 94587,** _____

Post Office Address _____

Full Name of Second Joint Inventor, if any _____

Second Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Third Joint Inventor, if any _____

Third Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Fourth Joint Inventor, if any _____

Fourth Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____